

UWB Oscillator Issues

For UWB System, Timing is of Crucial Importance

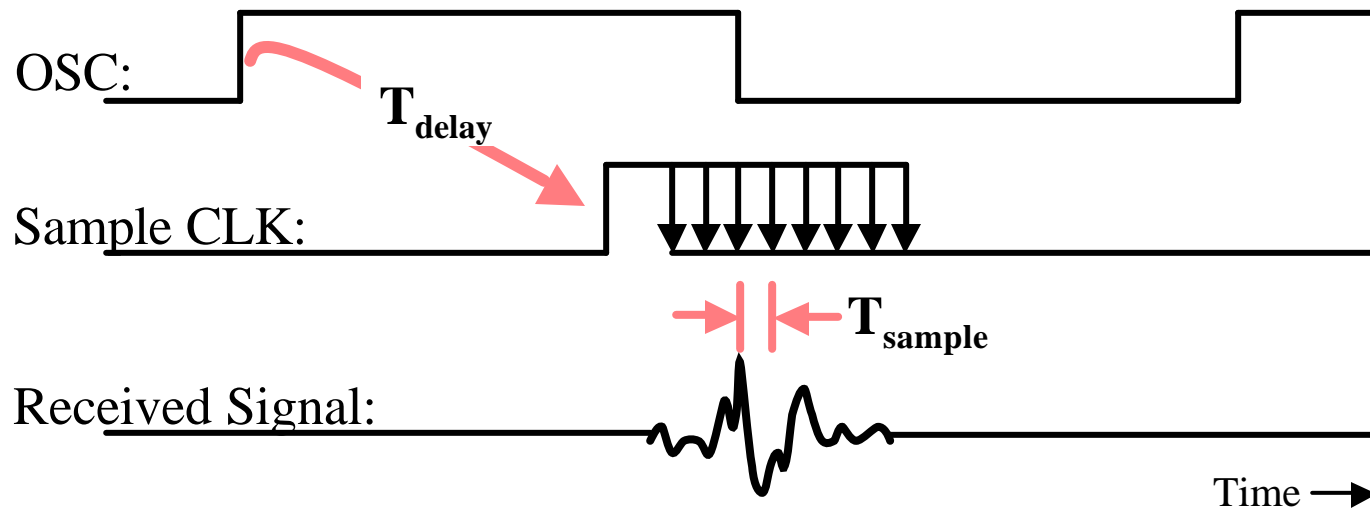
Transmit:

As pulses are on the order of a nanosecond, we need a stable, accurate reference to generate and position it within a much larger time window (on the order of a microsecond).

Receive:

In addition to the above criteria, we need to be able to track the pulse over a spread of N chips (on the order of N microseconds).

UWB Receiver Timing



Two Critical Timing Components:

- Reliable delay generation
- Accurate sampling

Oscillator Requirements

Accurate Pulse Repetition Frequency

f_{osc} match by better than +/-20ppm

Low Phase Noise (Low Jitter) Sampling

Overall jitter less than 0.1ns

(corresponds to -100dBc at 100kHz)

Low Power Operation

Power budget < 100 μ W

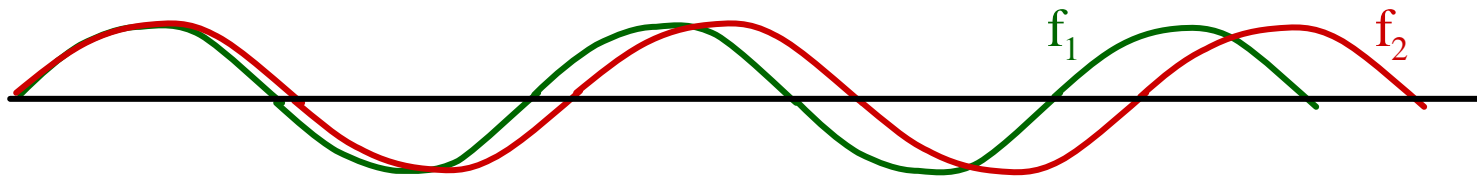
Low Cost, Integrated Solution

Ideally only need one external component

Point Towards a Crystal Implementation

Oscillator Accuracy

Mismatch Causes Drift:



**Number of Cycles to
Drift 'T' seconds:**

$$N = \frac{1}{2} \left(\frac{1 - \left(\frac{\Delta f}{f} \right)^2}{\frac{\Delta f}{f}} \right) f \cdot T$$

Define $f = (f_1 + f_2)/2$ and $\Delta f = |f_1 - f_2|$

**Based on Spreading and Bit-Rate, Can Calculate
Minimum Allowable Mismatch.**

Phase Noise/Jitter

Empirical Phase Noise Formula (in dB):

$$L\{\Delta\omega\} = 10 \log_{10} \left(\frac{2FkT}{P_{sig}} \left[1 + \left(\frac{\omega_o}{2Q\Delta\omega} \right)^2 \right] \left(\frac{1 + \Delta\omega / f_3}{|\Delta\omega|} \right) \right)$$

Relating to Jitter:

$$S_{\Delta T}^2 = L\{\Delta\omega\} \left(\frac{\Delta\omega}{\omega} \right)^2 T$$

S_{DT} proportional to $1/Q$

Implications: Desire high Q oscillator for low jitter.

Power Consumption

Power Trend:

Equating g_m from long channel model to requirement for oscillation (loop gain > 1), we can show:

$$I_{bias} > \left(\frac{1}{Q}\right)^2 (w_o C_p)^2 \left(\frac{C_1 + C_2}{C_1}\right)^2 \left(\frac{1}{2\mu C_{ox} W/L}\right)$$

I_{bias} proportional to w_o^2 , and $1/Q^2$

Implications:

Desire lowest possible operating frequency, and high Q .

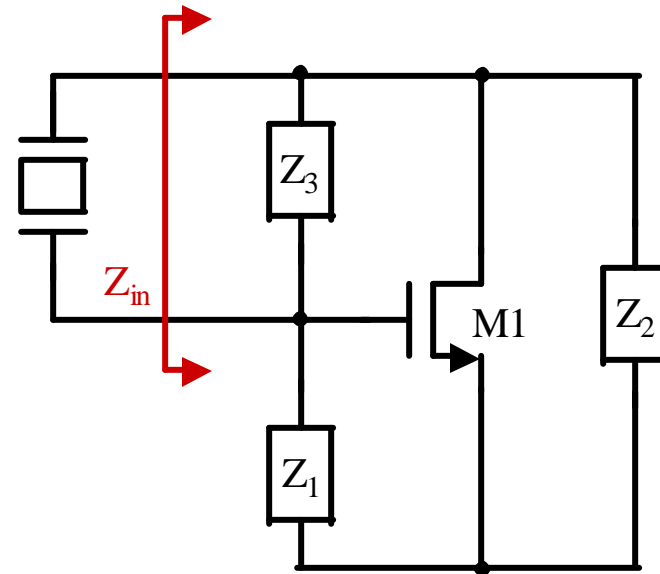
Pierce (“3-Point”) Oscillator

Preferred for Integrated, High-Precision Implementation

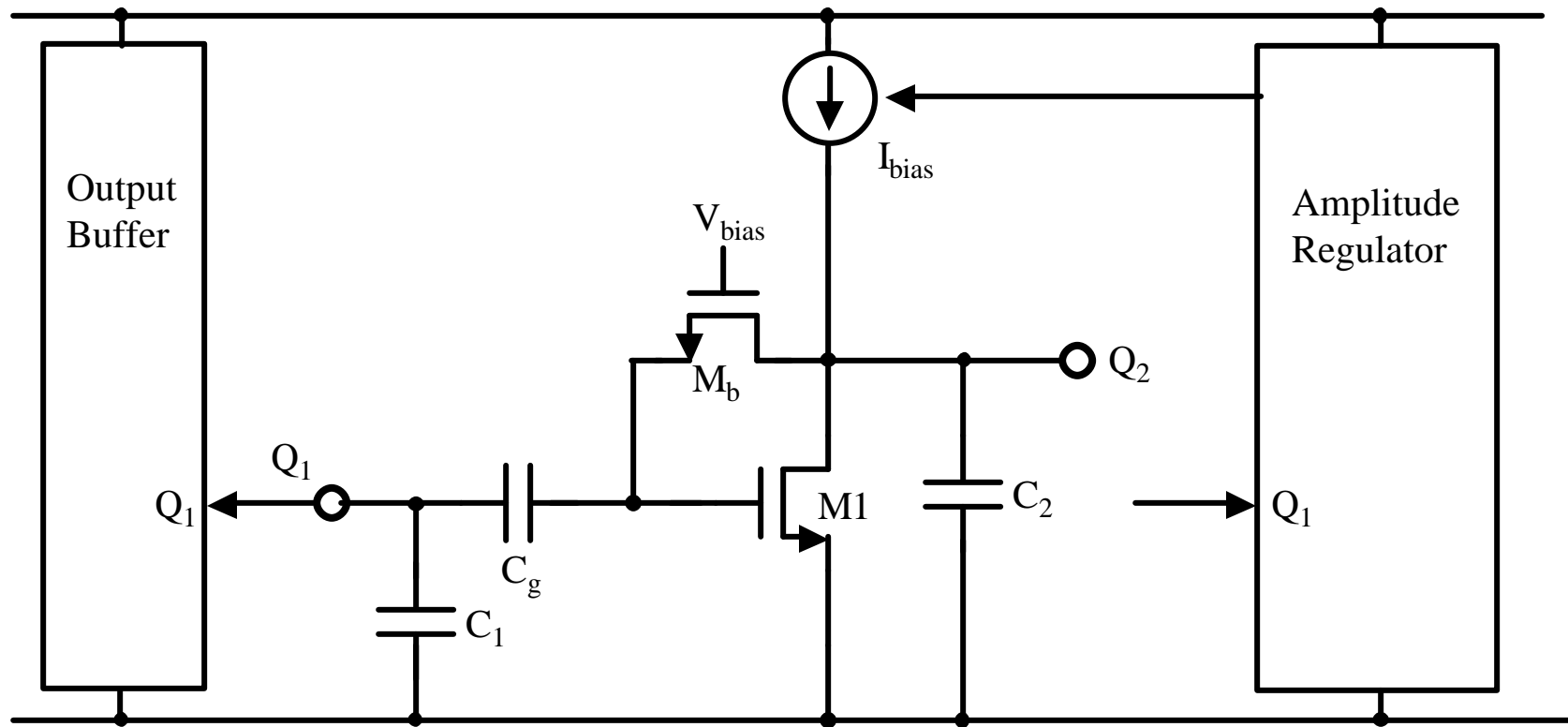
To Oscillate, Crystal Appears Inductive

ω_{osc} pulled by imaginary component of Z_{in}

$$p(\%) = -\text{Im}\{Z_{in}\} \left(\frac{\omega C_x}{2} \right)$$



Proposed Oscillator



Vittoz, E., Degrauwe, M., Bitz, S.; "High-Performance Crystal Oscillator Circuits: Theory and Application.", IEEE Journal of Solid-State Circuits, Vol. 23, No.3, June, 1988.

Continuing Work

Finish Timing Architecture and Start Circuit Design:

1. Sampling Edge Generation

Weigh power trade-off between frequency synthesis approach and single oscillator. I.e. Slower osc. with PLL/DLL vs. faster osc.

2. Window Delay Generation

Weigh power trade-off between accurate/tunable delay element and multiplexed edges from faster oscillator.