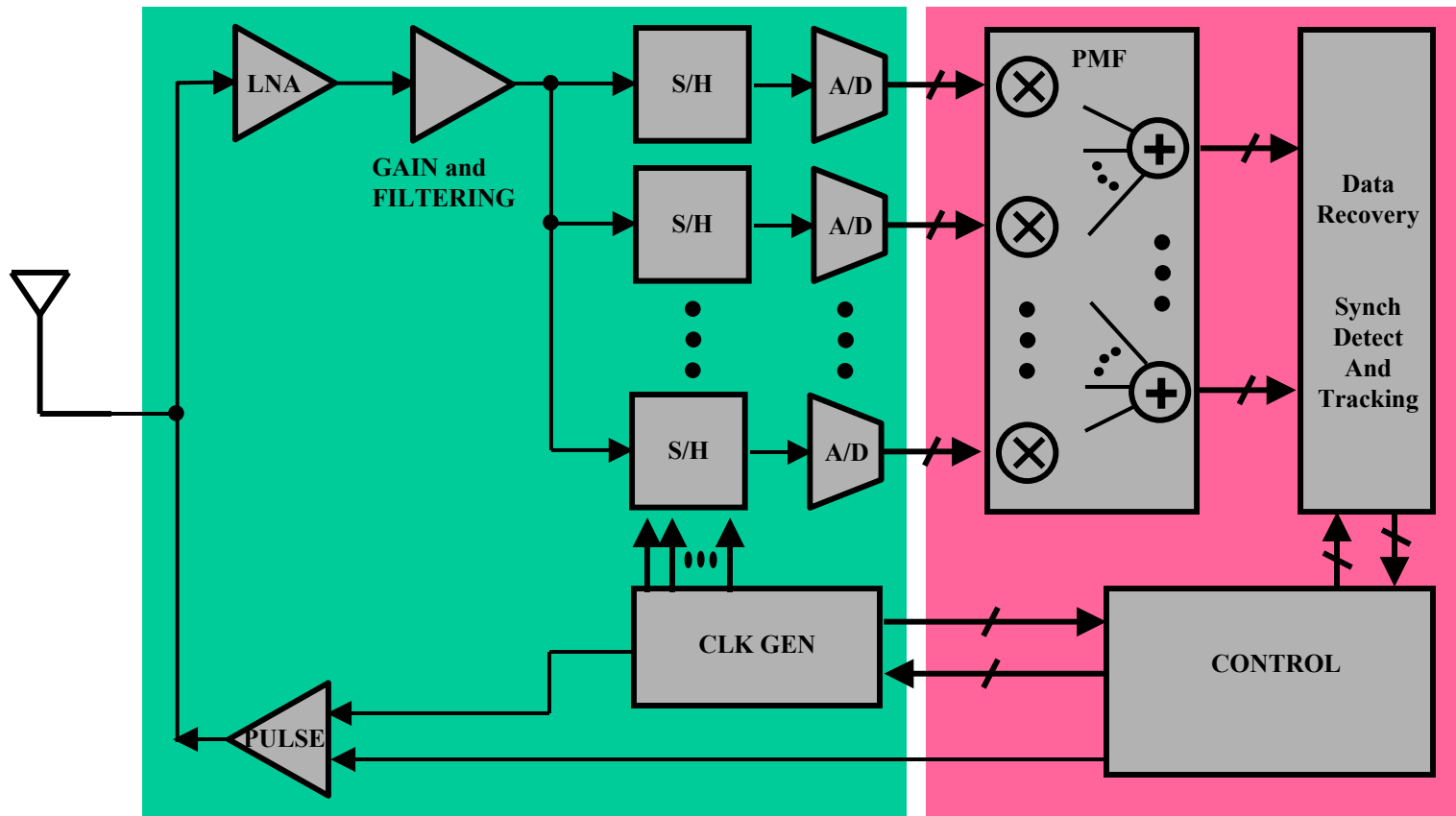


# UWB Transceiver Prototype

**Goal: Tape-out Single-Chip Transceiver by end of Summer**



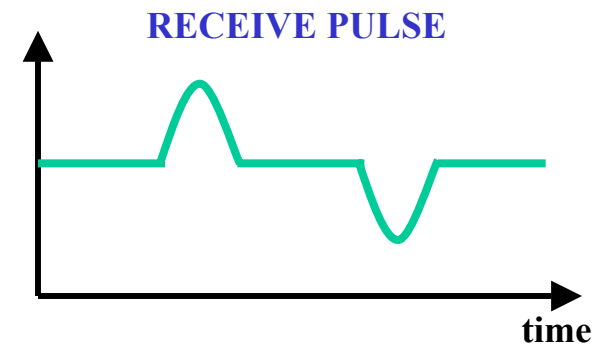
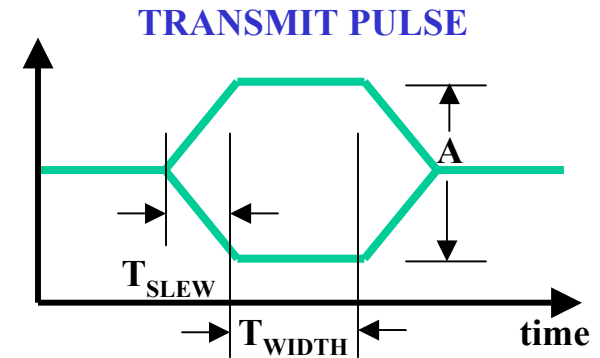
# TX: Pulse Transmitter

## Desirable Functionality:

- Adjustable Slew Rate and Width
- Variable Magnitude Drive (I or V)
- Ability to Drive High or Low Impedance
- Digitally Programmable
- PAM (Binary Antipodal), and PPM (2 to 4 Steps)

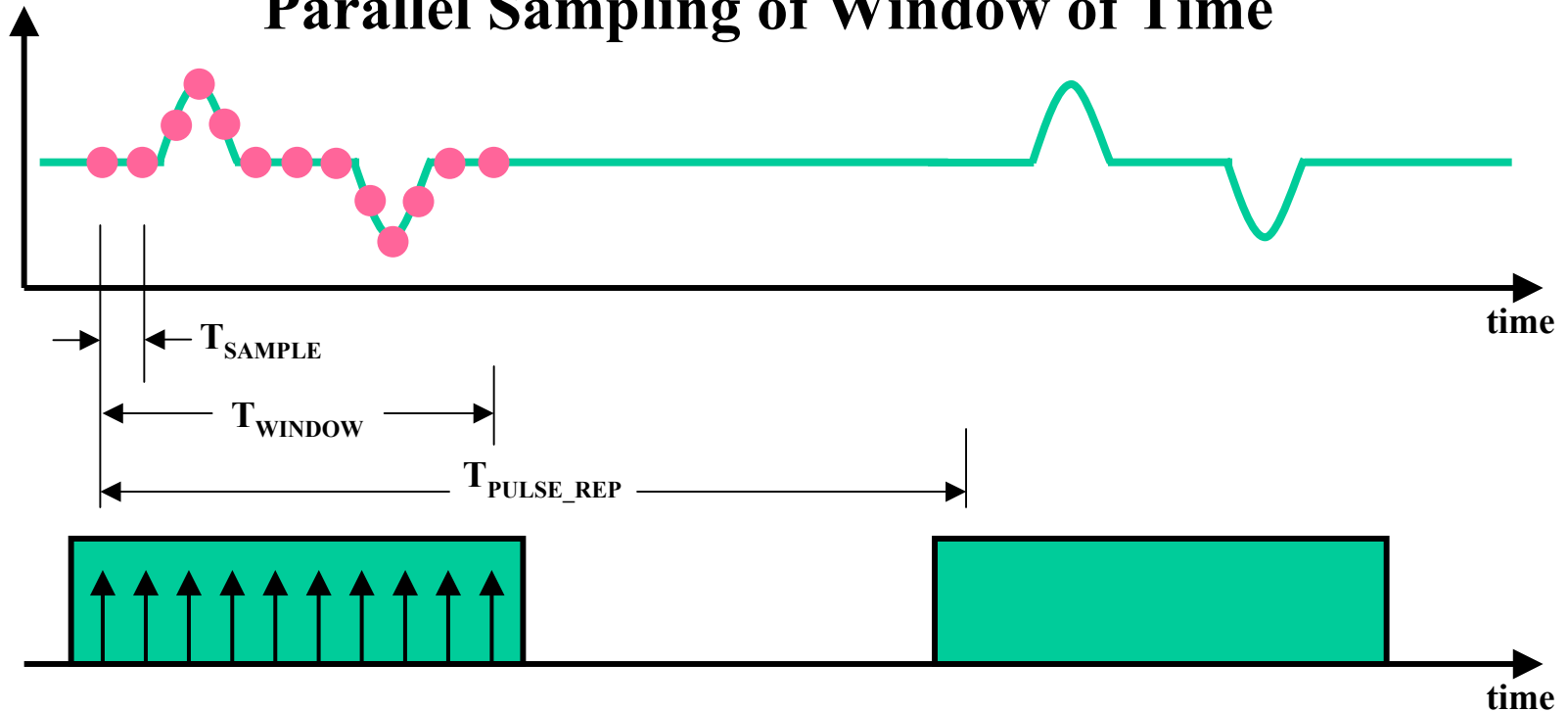
## Implementation:

Differential Drive for PAM  
Multiplex DLL Clock Phases to Control Width and for PPM  
May Build Two Drivers and Selectively Connect/Enable for Experimentation



# Pulse Reception

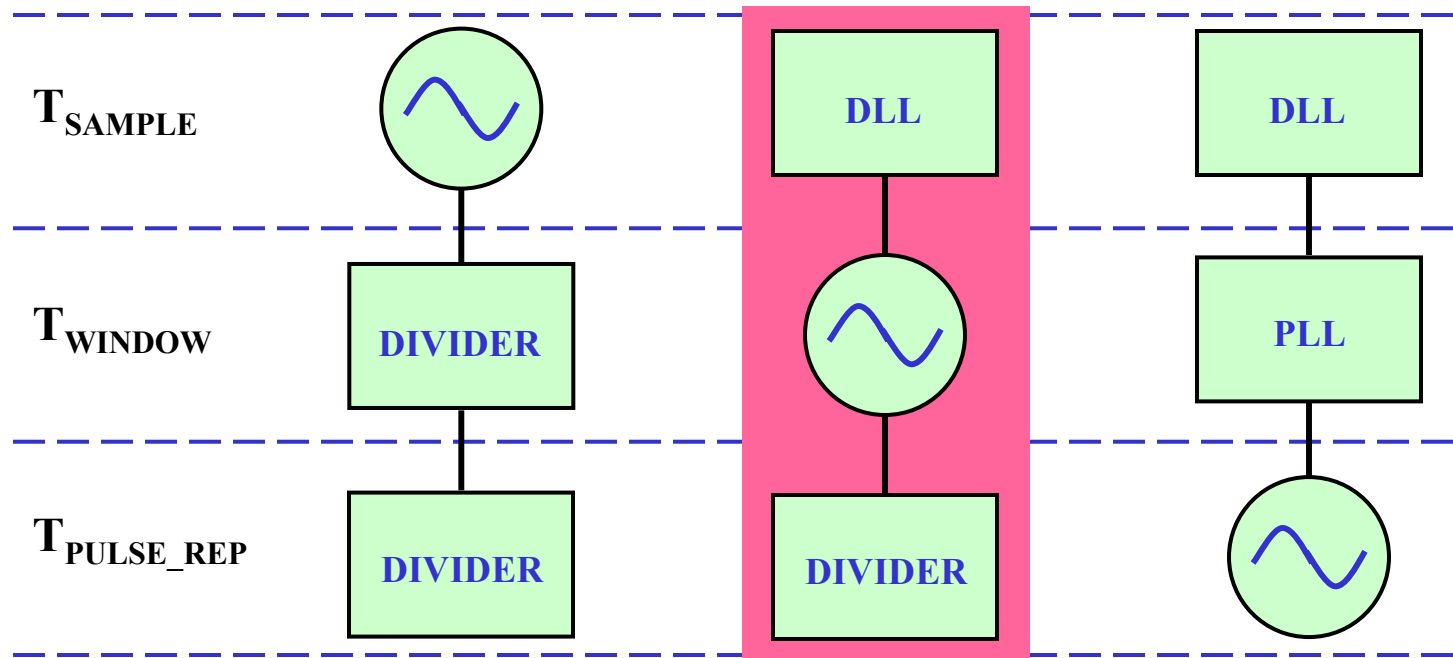
## Parallel Sampling of Window of Time



### Three Clocking Timescales:

$T_{\text{SAMPLE}}$  (<ns)     $T_{\text{WINDOW}}$  (~10's ns)     $T_{\text{PULSE\_REP}}$  (~100's ns)

# Oscillator Frequency



**For Lower Power: Base System Clock on  $T_{\text{WINDOW}}$**

$T_{\text{SAMPLE}}$  Derived from DLL

$$T_{\text{PULSE\_REP}} = T_{\text{WINDOW}} / N$$

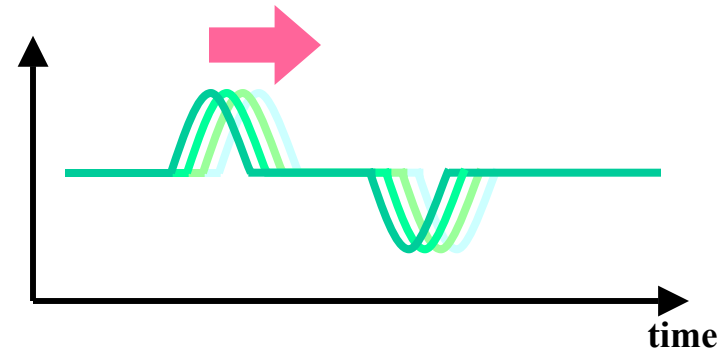
# Oscillator Accuracy

## Frequency Mismatch Causes Drift

Time to Slide One Sample Over One Received Bit; Given Mismatch, Pulse (Chip) Repetition Rate, and Length of PN Sequence.

$$\frac{\Delta f}{f} \approx \frac{1}{2} \left( \frac{T_{SAMPLE}}{N_{PN} \cdot T_{PULSE\_REP}} \right)$$

$$f = (f_{TX} + f_{RX})/2 ; \Delta f = (f_{TX} - f_{RX})$$



$$T_{SAMPLE} = 0.5ns$$

$$T_{PULSE\_REP} = 100ns$$

$$N_{PN} = 1024$$

$$T_{WINDOW} = 10ns$$

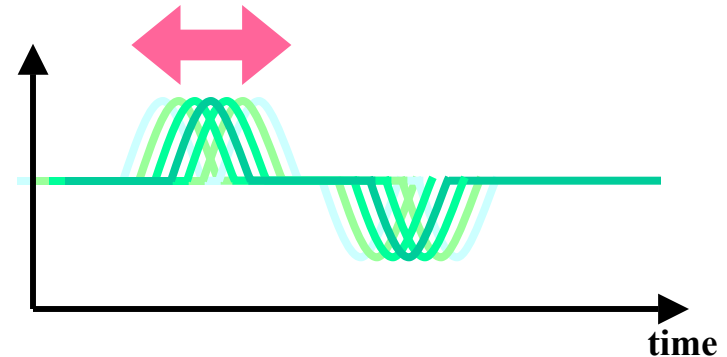
$$\Delta f/f = 2.4 \text{ PPM}$$

# Oscillator Jitter

## Phase Noise Bound:

Maximum Allowable Phase Noise for  $\sigma_{\Delta T} = 100\text{ps}$  (per Oscillator) Over the Reception of One Bit.

$$\mathcal{L}\left\{\frac{\Delta w}{w}\right\} = \left( \frac{\sigma_{\Delta T}^2}{(\Delta w / w)^2 \Delta T} \right)$$



$$T_{\text{SAMPLE}} = 0.5\text{ns}$$

$$T_{\text{PULSE\_REP}} = 100\text{ns}$$

$$N_{\text{PN}} = 1024$$

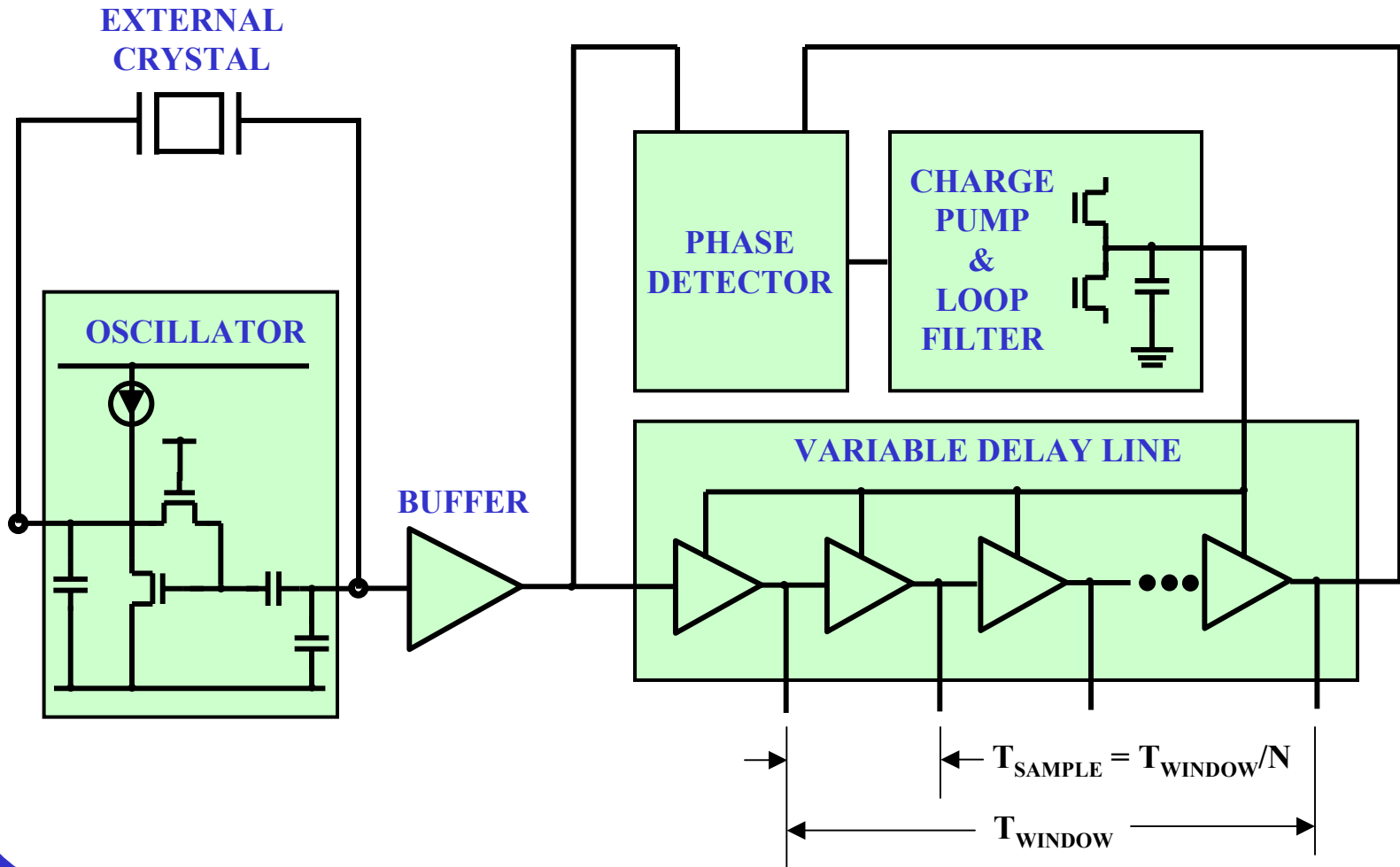
$$T_{\text{WINDOW}} = 10\text{ns}$$

$$\mathcal{L}\{100\text{kHz}/100\text{MHz}\}$$

$$= -100\text{dBc/Hz}$$

$$(\sigma_{\Delta T} = 100\text{ps})$$

# RX: Clock Generation



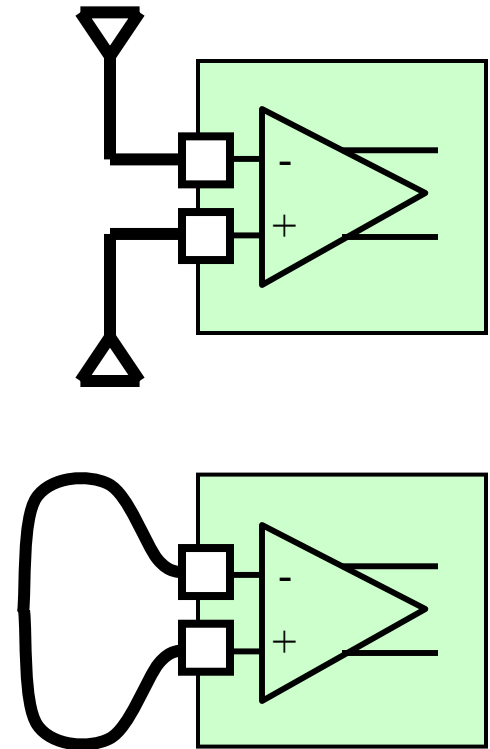
# RX: LNA

## Desirable Functionality:

- Gain  $\sim 10$  V/V over  $\sim 1$ GHz BW
- Noise Figure  $< 10$ dB (Not Critical In an Interference Dominated Environment)
- Differential Input
- Handle Multiple Antennas (I.e. Current Loop and/or Dipole)
- Switch Bias On/Off within  $T_{\text{WINDOW}}$
- Fast Overload Recovery (Track Full-Scale 1GHz Sinusoid)

## Implementation:

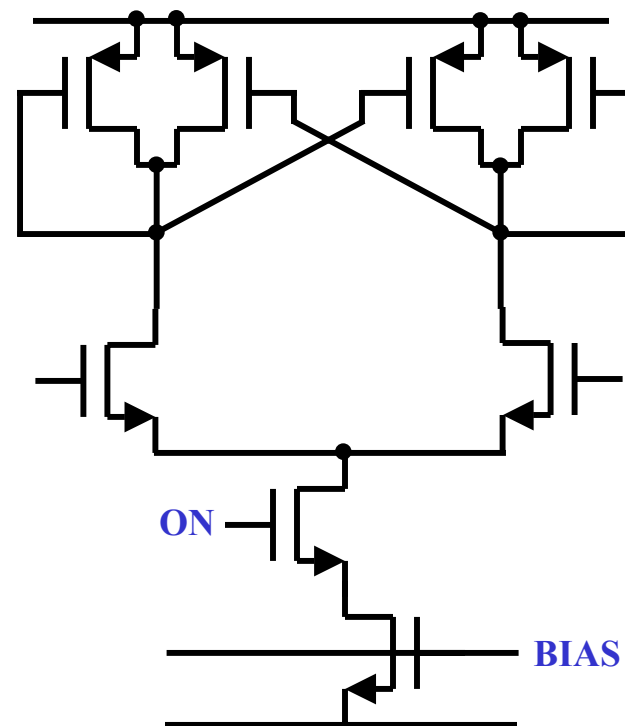
May Build Two Amplifiers and Selectively Connect/Enable for Experimentation



# RX: Gain + Filtering

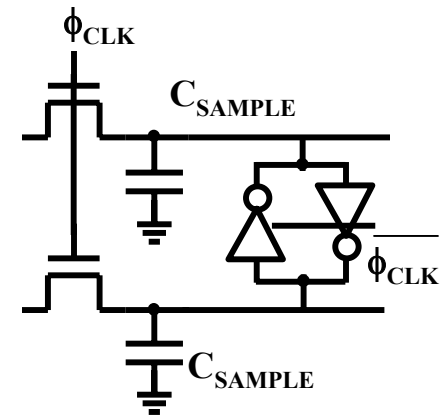
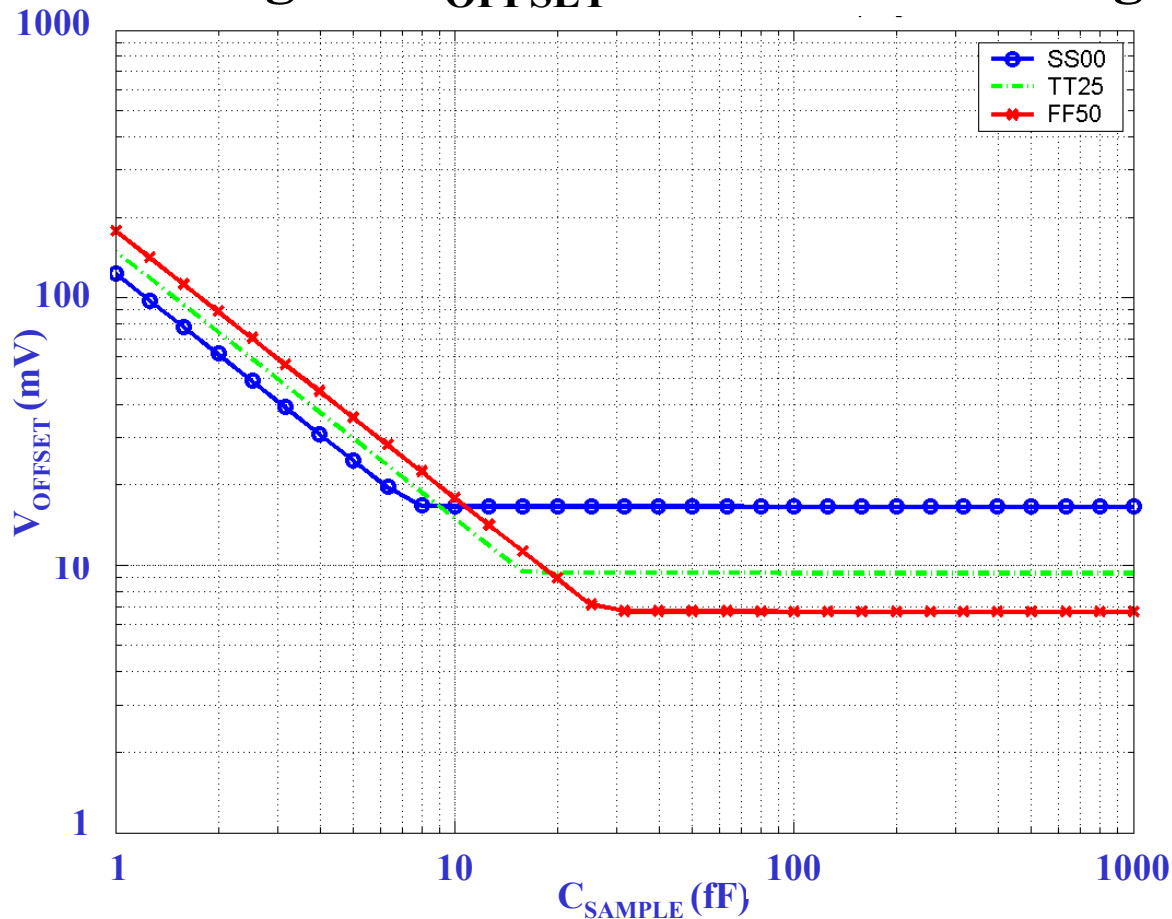
## Desirable Functionality:

- Minimum Gain = 1,000
- Partition Gain/Stages for Minimum Current Consumption
- Capacitive Coupling Between Stages (Null DC Offset)
- Switch Bias On/Off within  $T_{\text{WINDOW}}$
- Fast Overload Recovery (Track Full-Scale 1GHz Sinusoid)
- Additionally Include Filtering for Frequencies  $< 100\text{MHz}$ ,  $> 1\text{GHz}$
- Last Stage Drives Sampling Switch Load (could be  $\sim 100$ 's fF)



# RX: A/D Comparator

## 1-Sigma $V_{\text{OFFSET}}$ for Fixed Tracking BW=1GHz



$V_{\text{OFFSET}} \sim 20\text{mV}$   
(w/ No Explicit  
Cancellation) for  
 $C_{\text{SAMPLE}} > 10\text{fF}$