

UWB Transceiver Prototype

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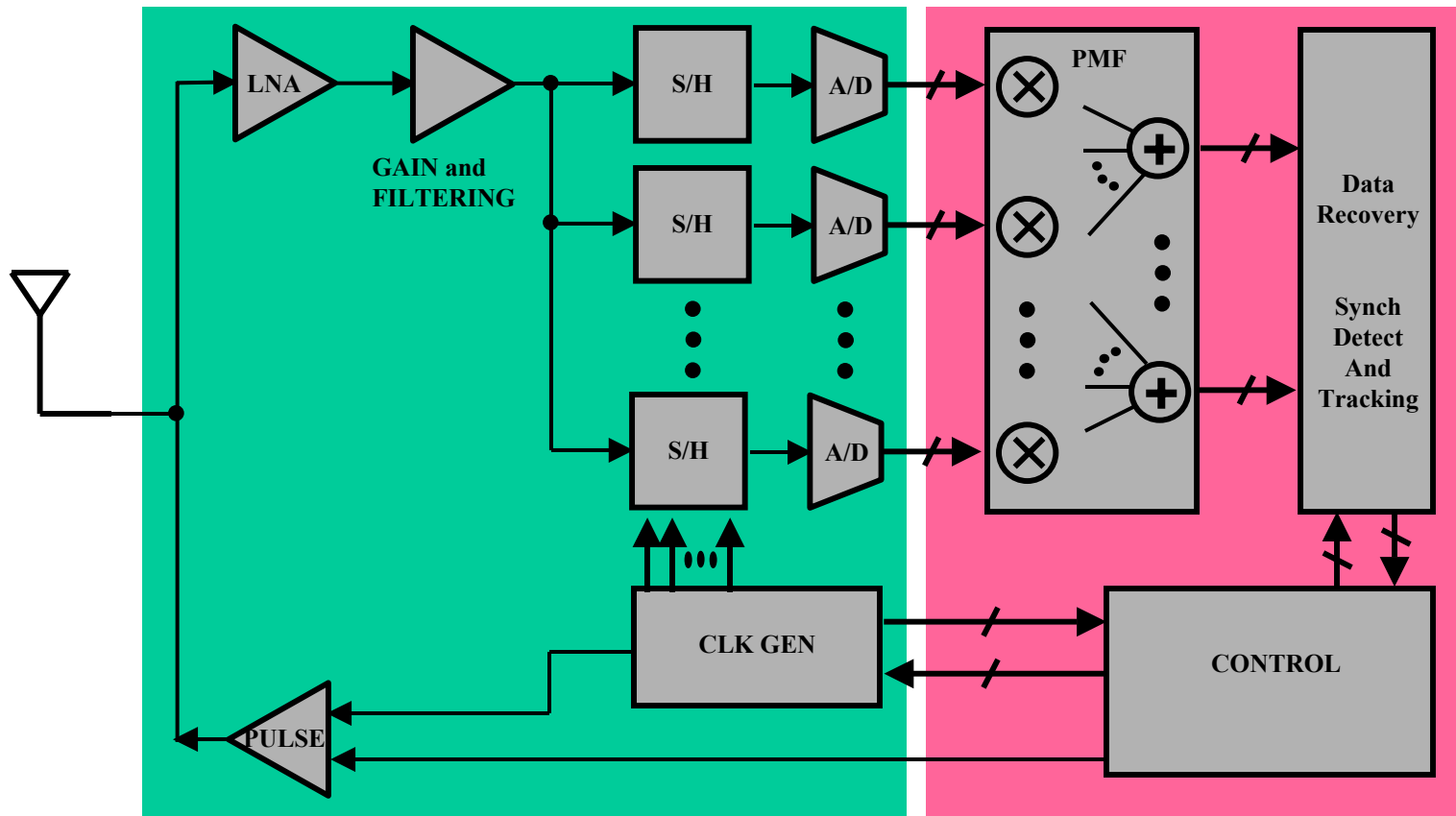
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Flexibility for UWB Design Exploration

- Different antennas (with impedance matching to the LNA)
- Variable transmit power
- Variable pulse rates
- Digital back-end will contain a programmable pulse-matched filter
- Adjustable data recovery/synchronization blocks
- Independent synchronization and data PN sequences
- I/O to send the A/D data directly to an external digital backend (i.e. BEE) for more sophisticated signal processing.

UWB Transceiver Prototype

Goal: Tape-out Single-Chip Transceiver by end of Summer



Pulse Transmitter

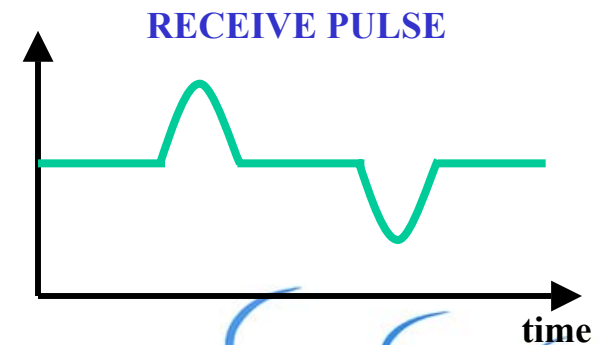
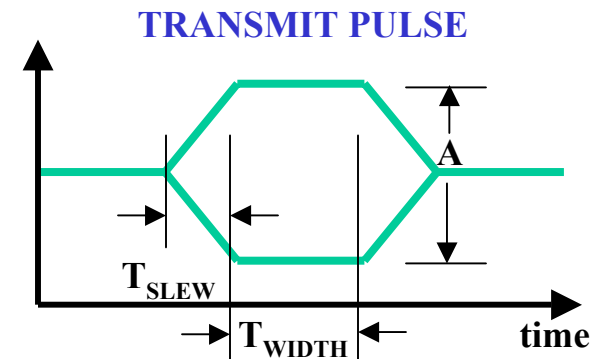
Pulse Transmitter

Desirable Functionality:

- Adjustable Slew Rate and Width
- Variable Magnitude Drive (I or V)
- Ability to Drive High or Low Impedance
- Digitally Programmable
- PAM (Binary Antipodal), and PPM (2 to 4 Steps)

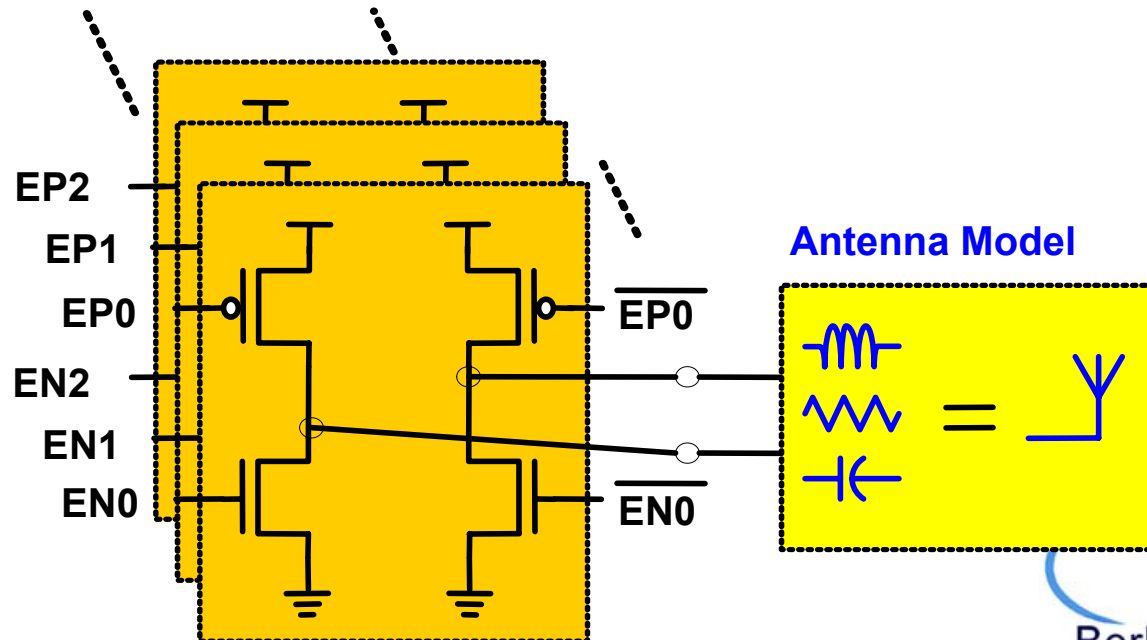
Implementation:

Differential Drive for PAM
Multiplex DLL Clock Phases to Control Width and for PPM
May Build Two Drivers and Selectively Connect/Enable for Experimentation



Flexible Antenna Driver

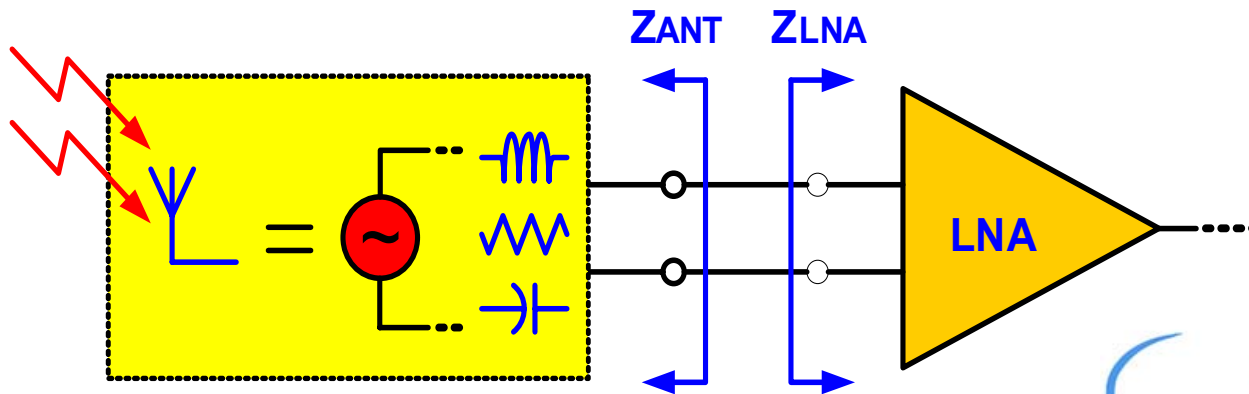
- Put the antenna circuit model into circuit simulator to design the driver
- H-bridge configuration
- Put them in parallel to make the driver flexible



Antenna-LNA Co-design

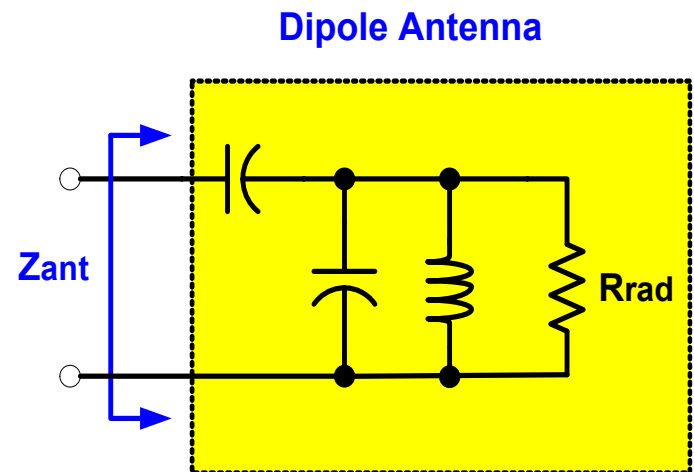
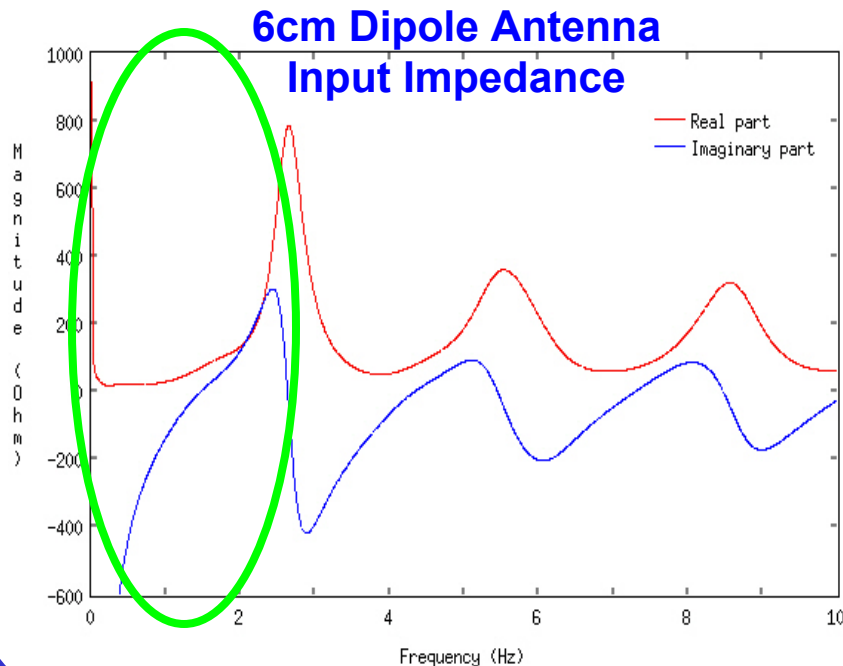
Antenna/LNA Co-design

- Impedance of the RX antenna seen by LNA is the same as that of the TX antenna
- Optimize LNA by putting the antenna model in front
- Usually voltage-drive RX antennas prefer large Z_{LNA} and current-drive antennas prefer small Z_{LNA}



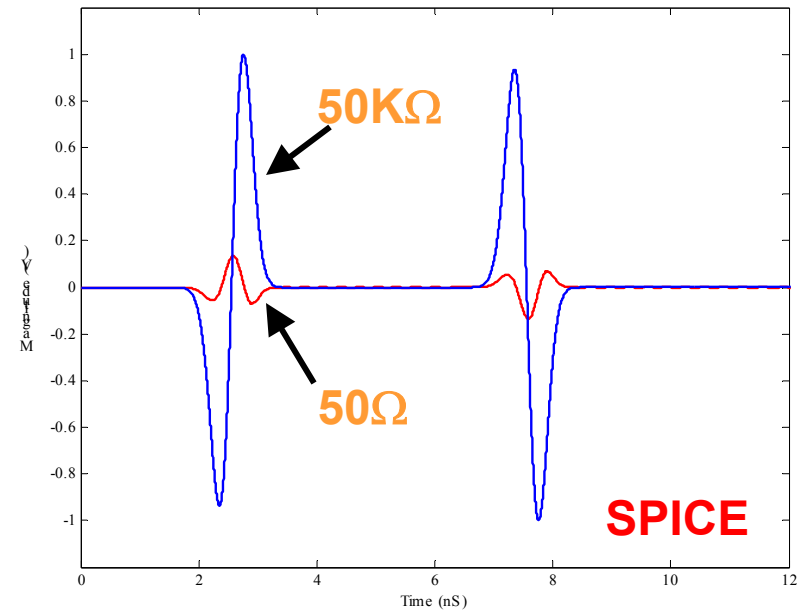
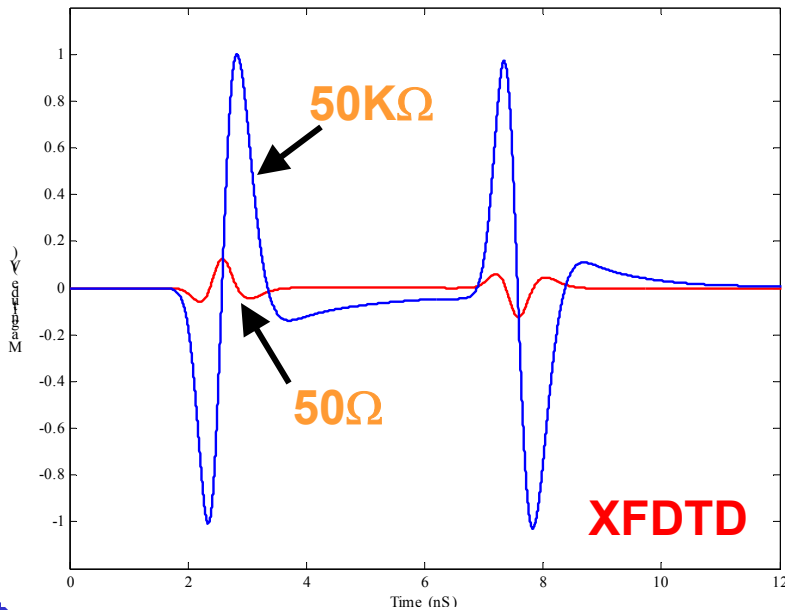
Equivalent Circuits for UWB Antennas

- Derive input impedance by simulations [U. Mass]
- Voltage-drive antenna will be capacitor-dominant while current-drive antenna will be inductor-dominant



Example: Monopole RX Antennas

- 2cm monopole antenna with different loading
- Larger Z_{LNA} gives higher LNA input voltage
- Mismatch due to scattering and near-zone field
- The relative magnitudes are close



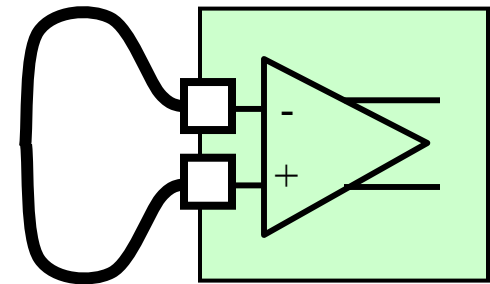
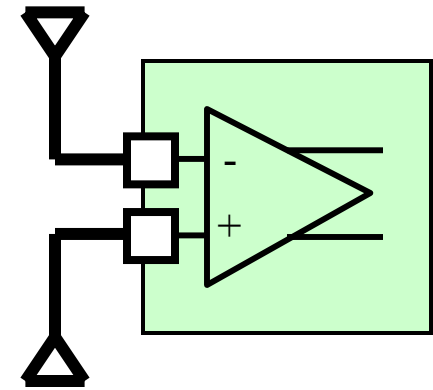
RX: LNA

Desirable Functionality:

- Gain ~ 10 V/V over ~ 1 GHz BW
- Noise Figure < 10 dB (Not Critical In an Interference Dominated Environment)
- Differential Input
- Handle Multiple Antennas (I.e. Current Loop and/or Dipole)
- Switch Bias On/Off within T_{WINDOW}
- Fast Overload Recovery (Track Full-Scale 1GHz Sinusoid)

Implementation:

May Build Two Amplifiers and Selectively Connect/Enable for Experimentation

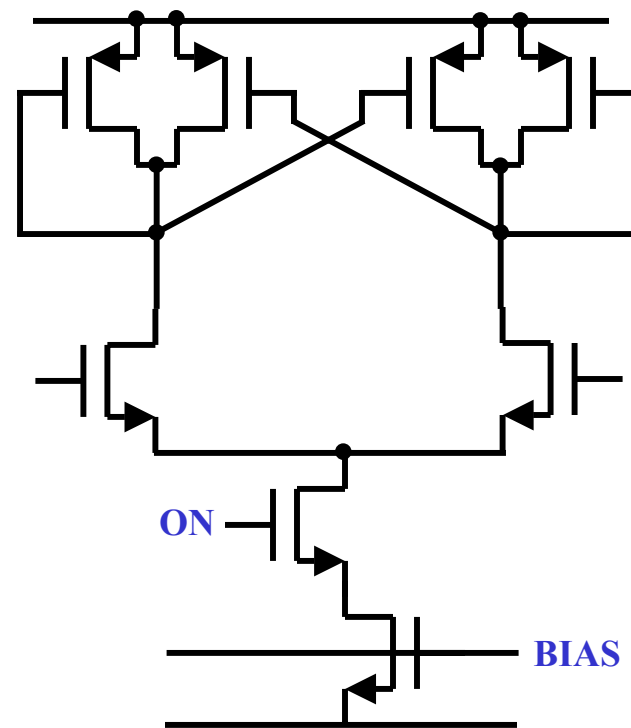


CMOS Analog Frontend

RX: Gain + Filtering

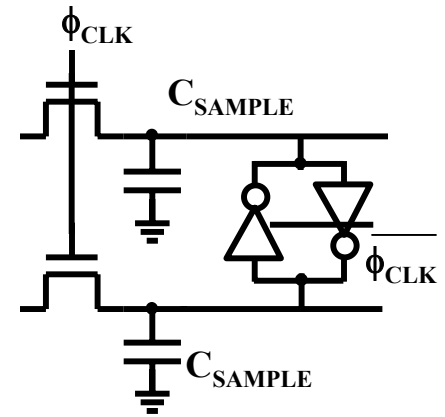
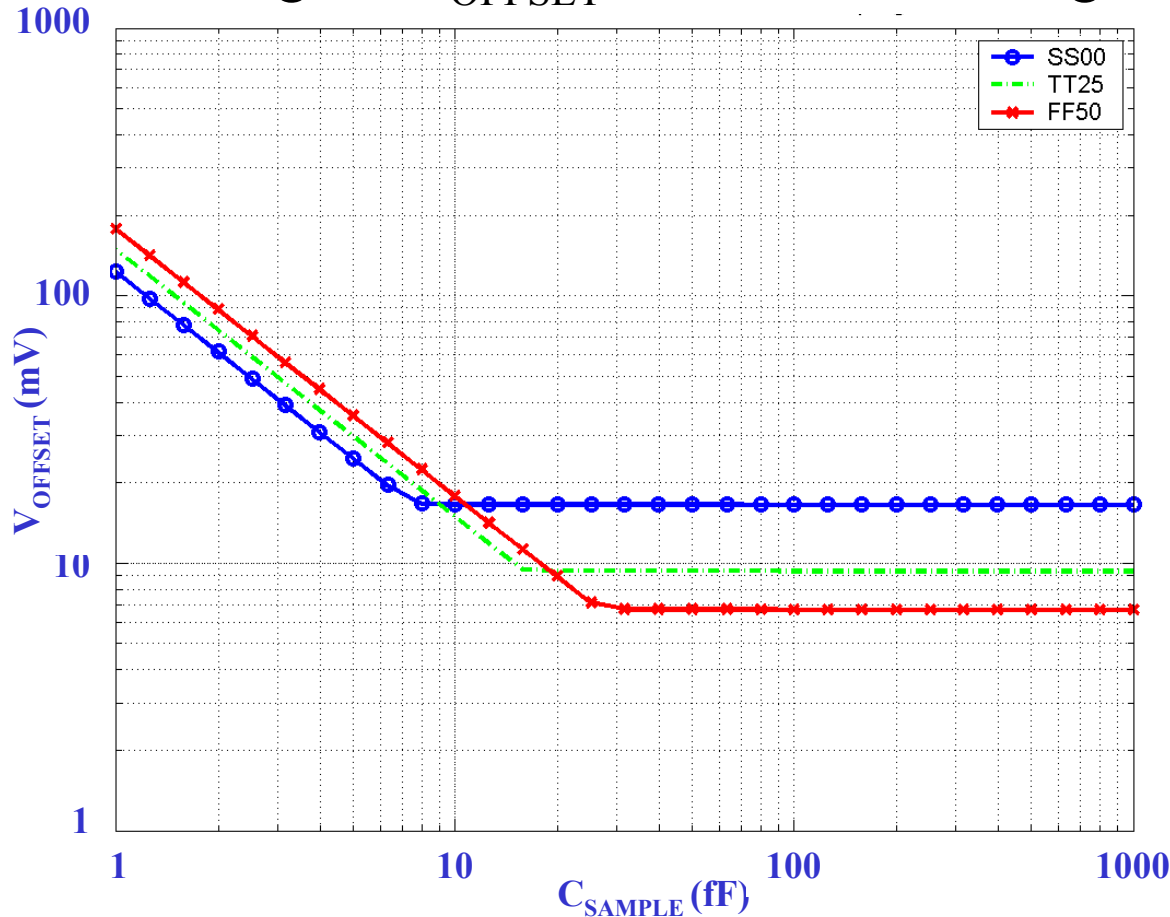
Desirable Functionality:

- Minimum Gain = 1,000
- Partition Gain/Stages for Minimum Current Consumption
- Capacitive Coupling Between Stages (Null DC Offset)
- Switch Bias On/Off within T_{WINDOW}
- Fast Overload Recovery (Track Full-Scale 1GHz Sinusoid)
- Additionally Include Filtering for Frequencies $< 100\text{MHz}$, $> 1\text{GHz}$
- Last Stage Drives Sampling Switch Load (could be ~ 100 's fF)



RX: A/D Comparator Requirement

1-Sigma V_{OFFSET} for Fixed Tracking BW=1GHz

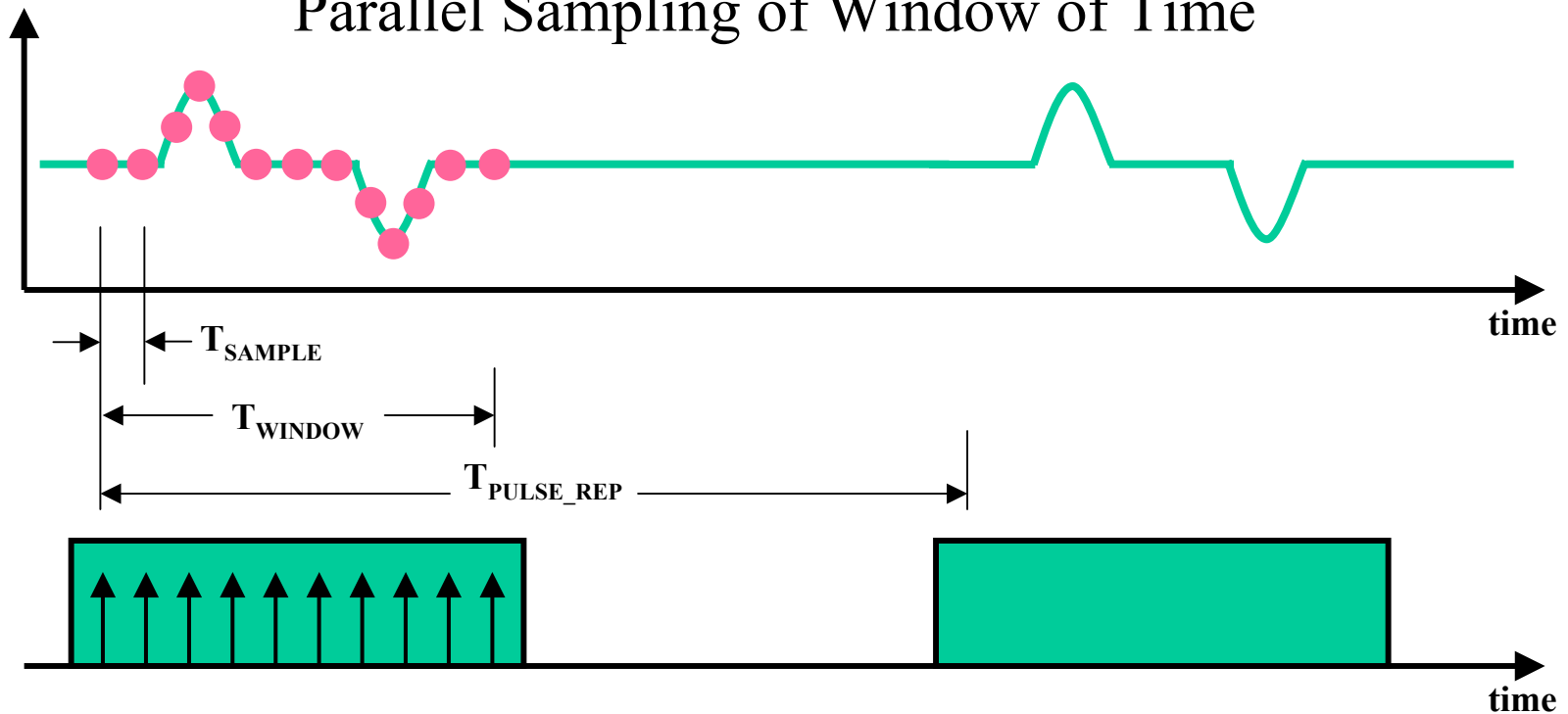


$V_{\text{OFFSET}} \sim 20\text{mV}$
(w/ No Explicit
Cancellation) for
 $C_{\text{SAMPLE}} > 10\text{fF}$

Clock Generation

Pulse Reception

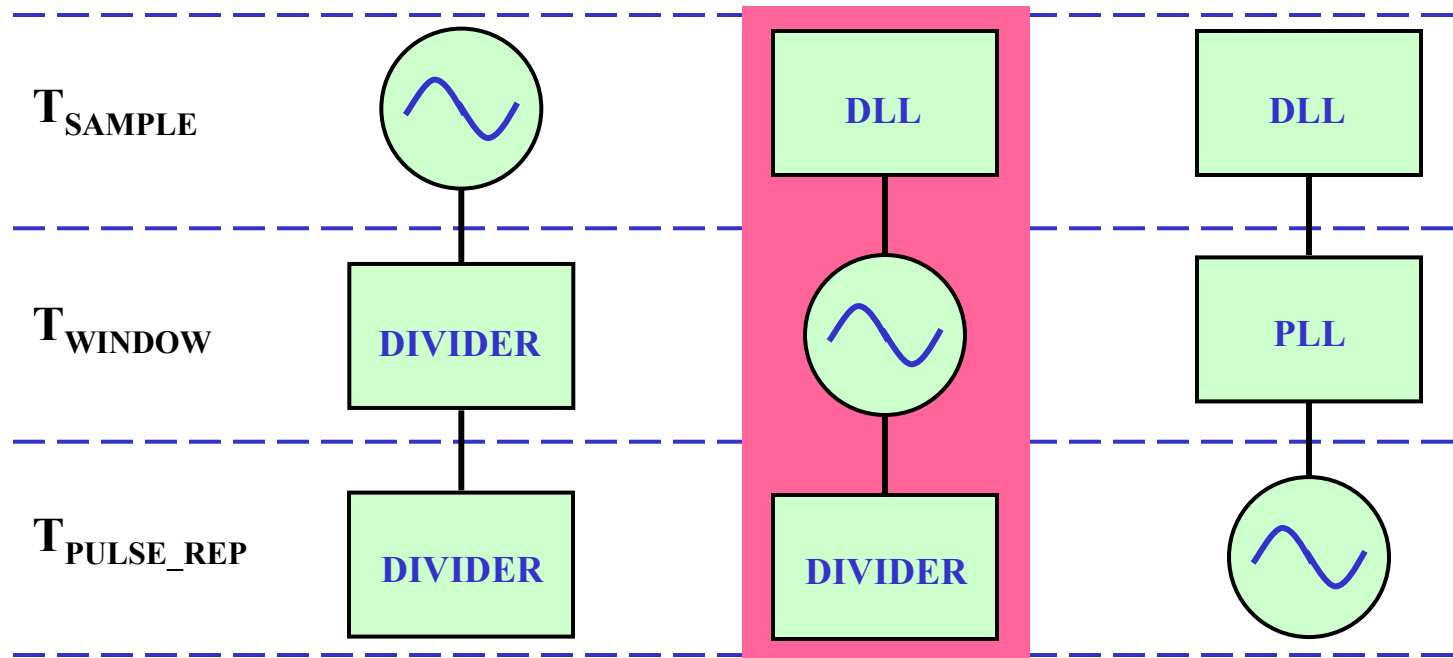
Parallel Sampling of Window of Time



Three Clocking Timescales:

T_{SAMPLE} (<ns) T_{WINDOW} (~10's ns) $T_{\text{PULSE_REP}}$ (~100's ns)

Timing Generation

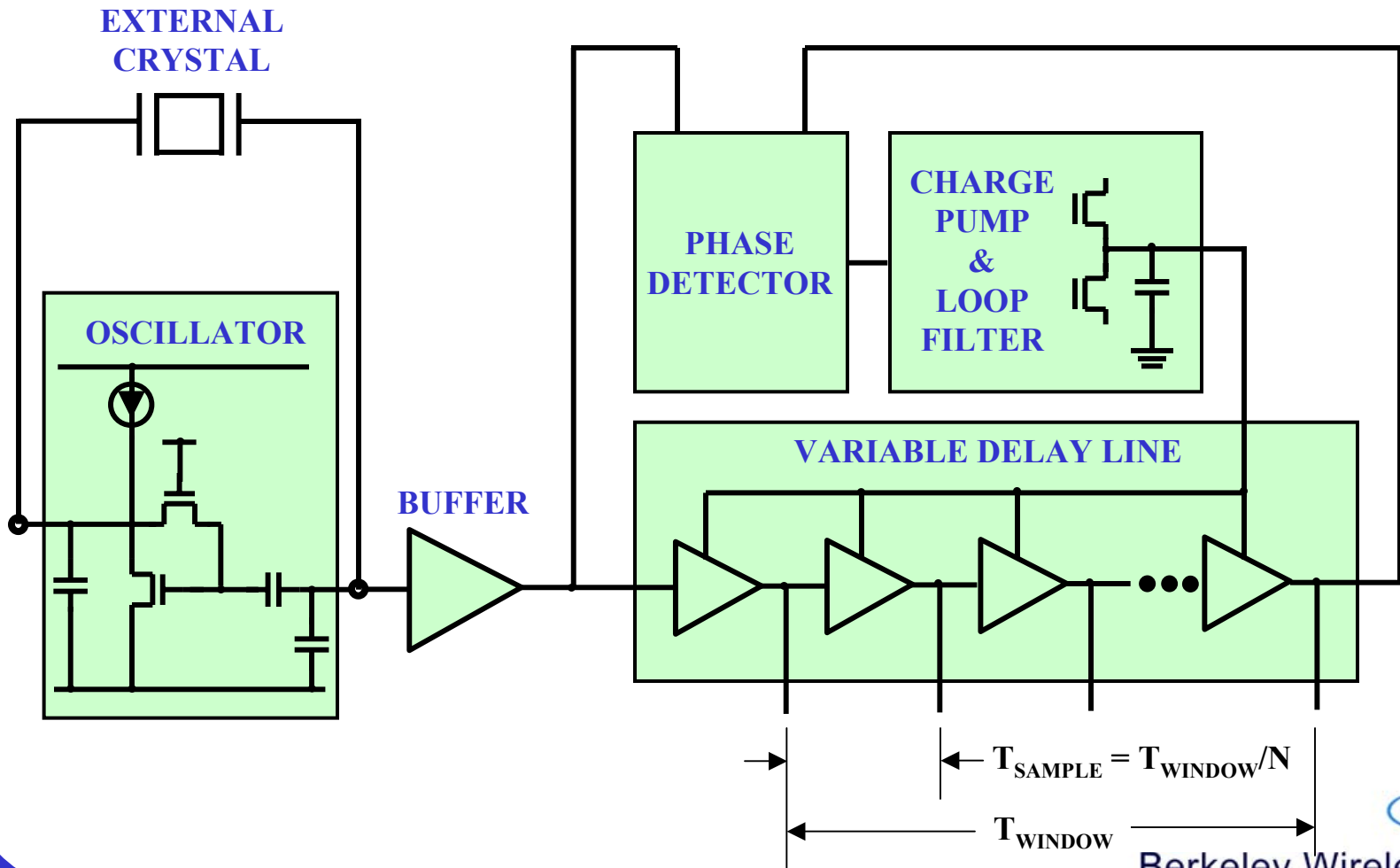


For Lower Power: Base System Clock on T_{WINDOW}

T_{SAMPLE} Derived from DLL

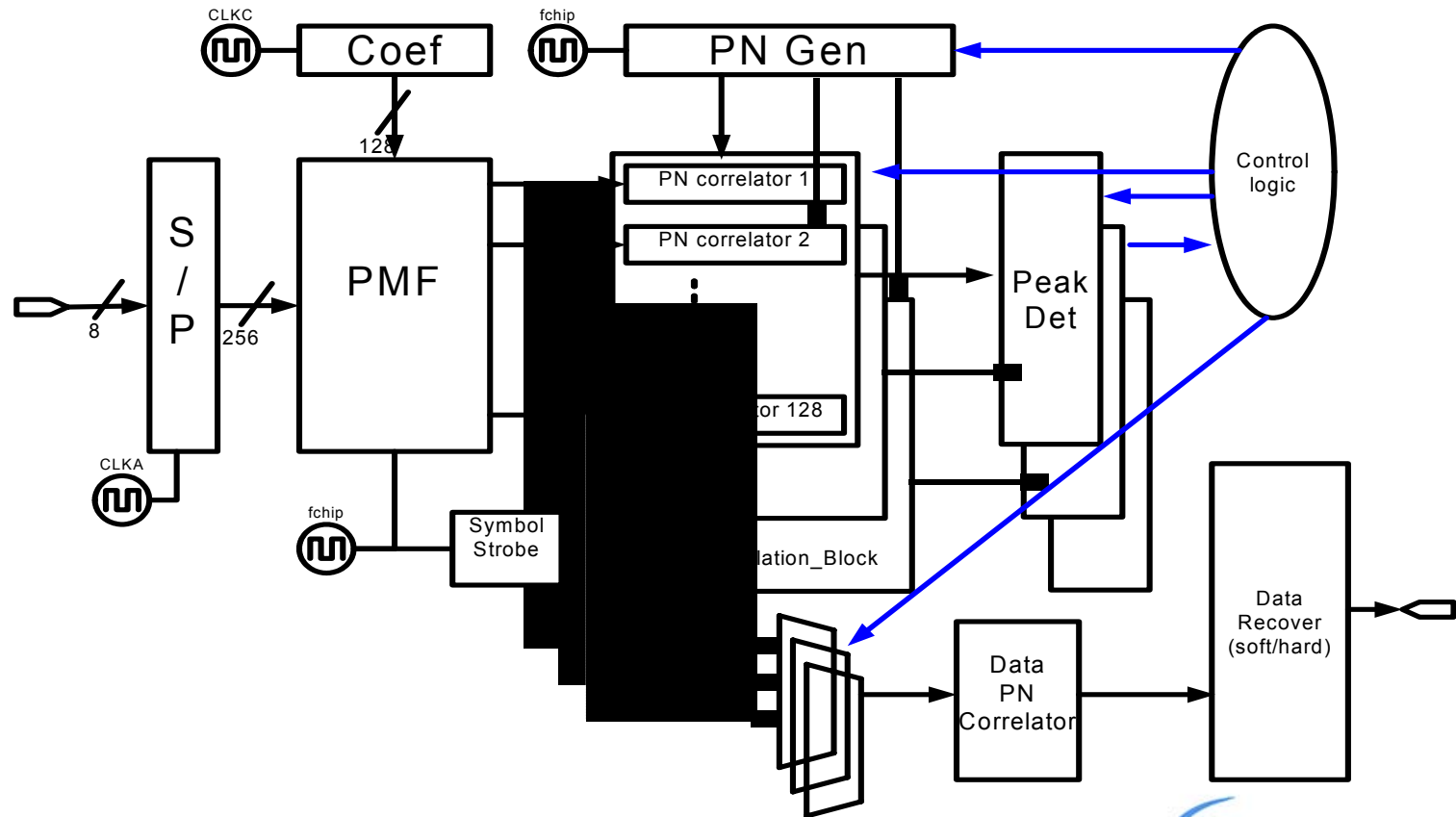
$$T_{\text{PULSE_REP}} = T_{\text{WINDOW}} / N$$

RX: Clock Generation



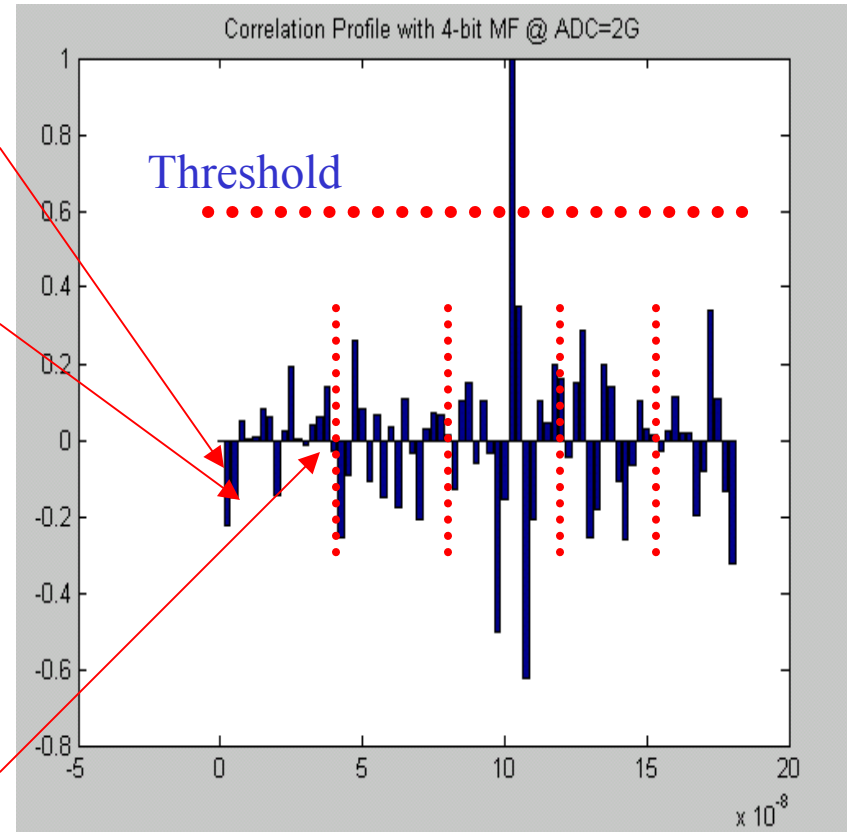
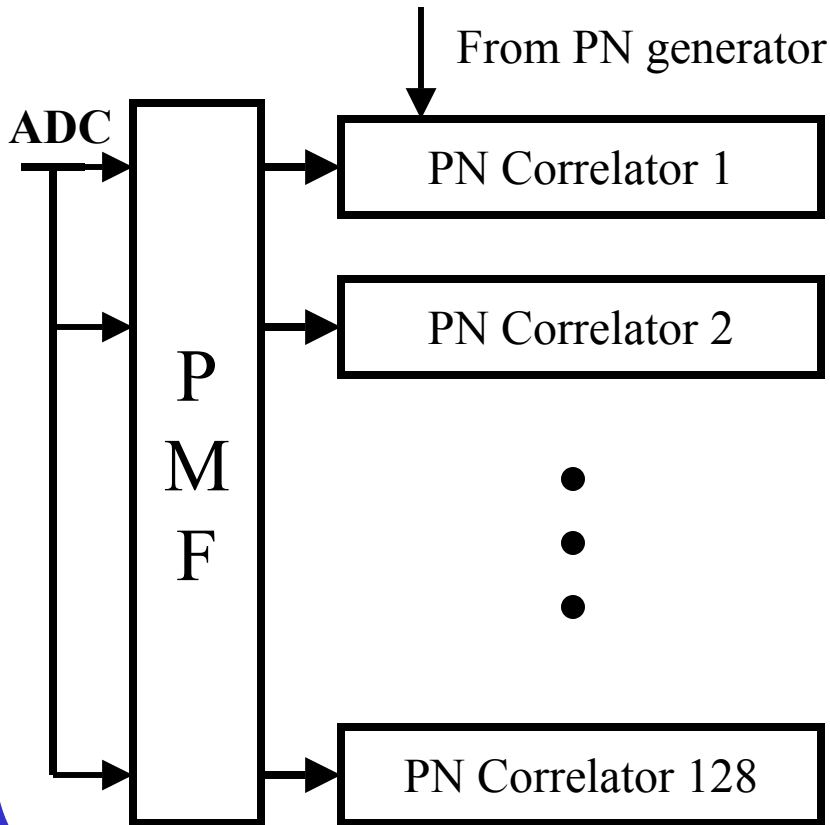
Overview of UWB Baseband

Baseband Overview

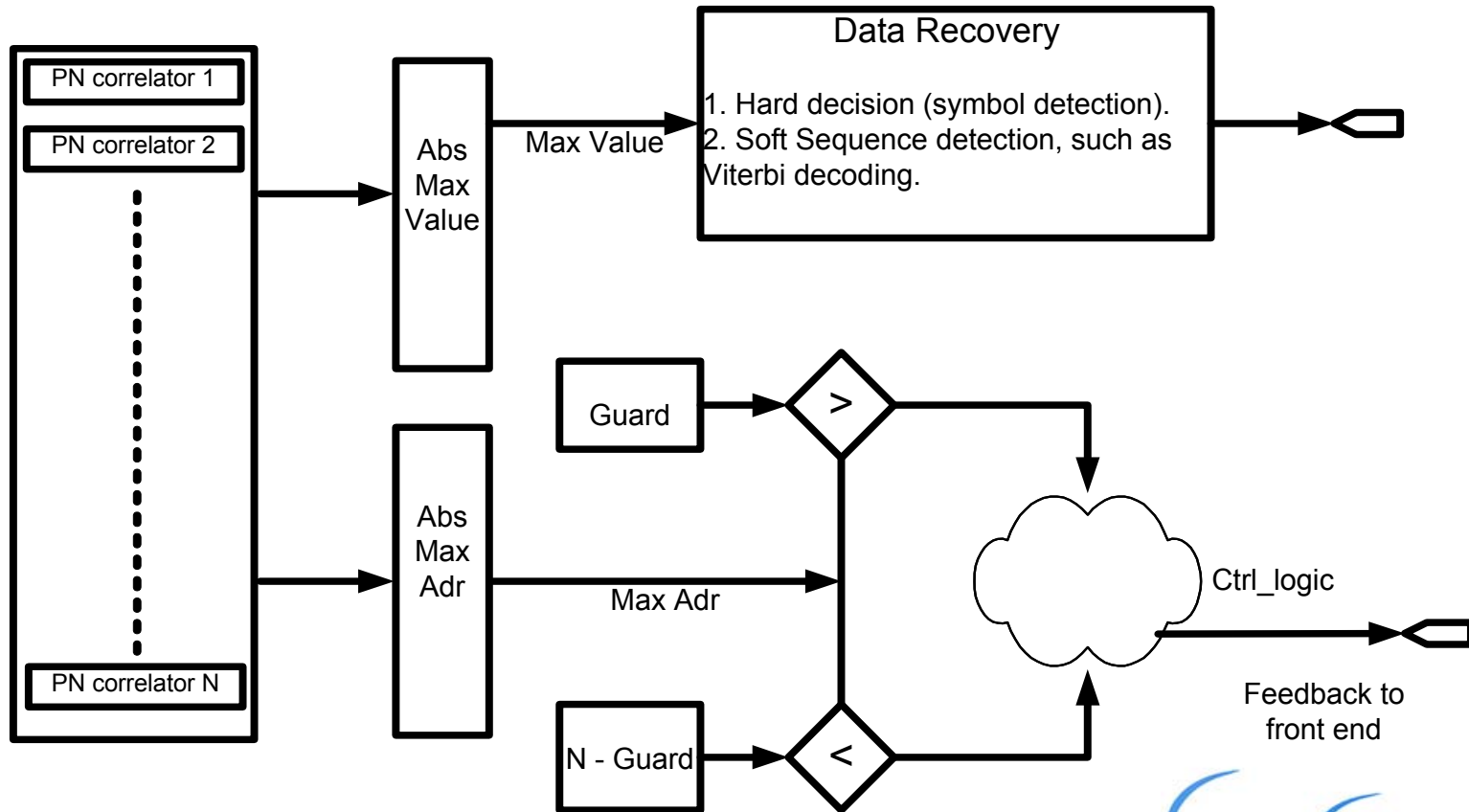


Acquisition Mode

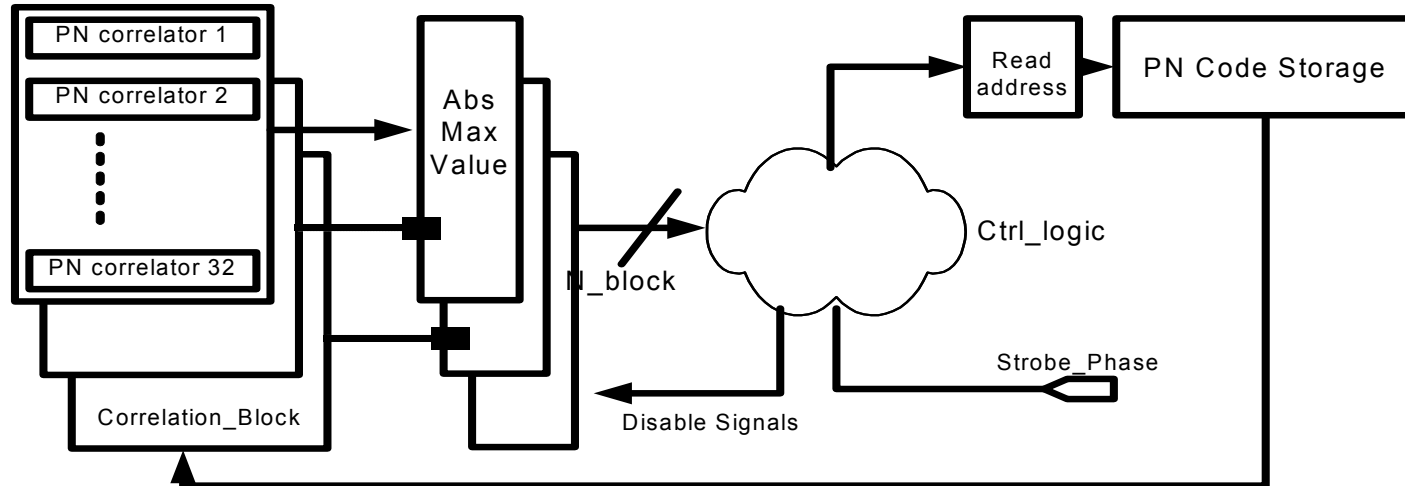
- Searching for the peak at the output of correlators



Tracking Mode

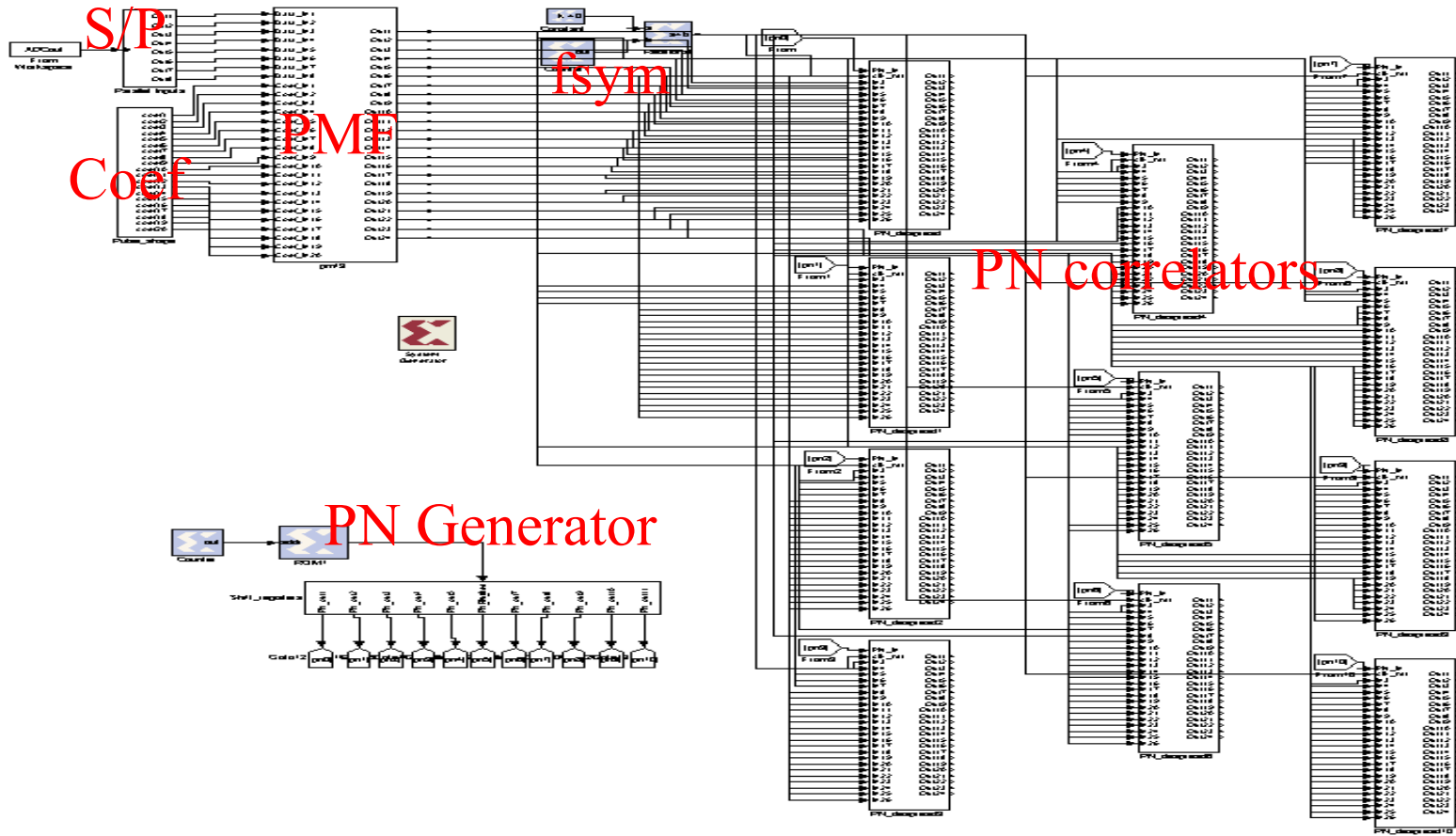


Control Logic



- A read clock to fetch the PN phase and a programmable PN length is needed.
- Strobe_phase signal is used to define the symbol boundary after entering tracking mode.
- A enable/disable control bus is needed for gated clock in PN correlators for power saving purpose.

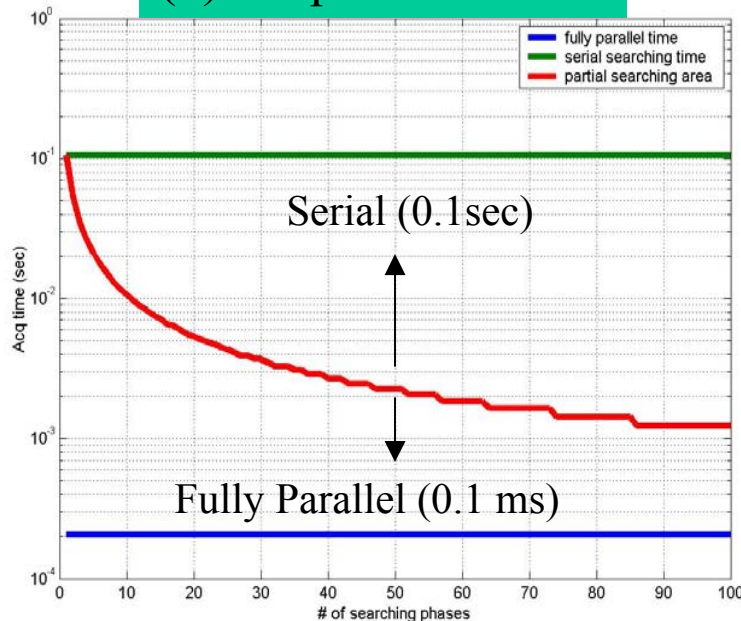
Simulink Implementation



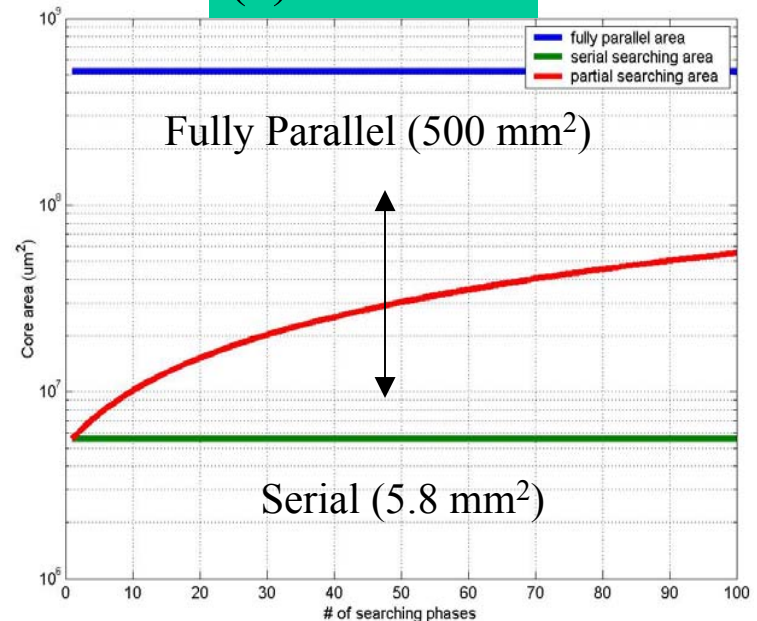
Parallel vs. Serial Acquisition

Assume the worst case using 1024 PN chips, while pulse rate is equal to 100 ns. We need to choose somewhere in between.

(1) Acquisition Time



(2) Area Cost



Area Distribution of Digital Backend

- The biggest single block is PMF(Pulse Matched Filter), which is implemented in Carry-save adders.
- PN correlators and Peak detectors are proportional to the number of searching phases. The optimal point makes this area comparable to PMF.

